No Input Electrolytic Capacitor Required, IEC61000-3-2 Class-C Isolated LED Driver IC

LC5540LD Series

Data Sheet

Description

The LC5540LD series are isolated LED drivers in which a power MOSFET and a control IC are highly integrated.

The IC provides the systems that can comply with the harmonics standard (IEC61000-3-2 Class C) in all conditions, including a light load condition. These systems, moreover, can be achieved without an input electrolytic capacitor.

The IC employs the average current and quasi-resonant controls: the average current control realizes high power factors, whereas the quasi-resonant control contributes to high efficiency and low noise.

Having a rich set of protection features, the IC can provide and more cost-effective power supply systems with fewer external components.

Features

- Built-in On-time Control Circuit
  (High Power Factor Achieved by Average Current Control)
- Built-in Startup Circuit
  (Reduced Numnber of External Components)
- Soft Start Function
  (Startup Stress Reduction for Power MOSFET and Secondary Rectifier Diode)
- Bias Assist Function
  (Improved Startup Performance, V_{CC} Voltage Drop Suppresion in Operation, Reduced Capacitance of VCC Pin Capacitor)
- Leading Edge Blanking Function
- Built-in Maximum On-time Limitation Function
- Protections Include:
  Overcurrent Protection (OCP): Pulse-by-Pulse
  Overvoltage Protection (OVP): Latched Shutdown
  Overload Protection (OLP): Latched Shutdown
  Thermal Shutdown (TSD): Latched Shutdown

Package

DIP8

Not to scale

Selection Guide

- **Electrical Characteristics**

Part Number	V_{DSS} (min.)	f_{OSC} (typ.)	$t_{ON(MAX)}$ (typ.)
LC5545LD	650 V	72 kHz	9.3 µs
LC5546LD		60 kHz	11.2 µs

- **Power MOSFET On-resistance and Output Power**

Part Number	$R_{DS(ON)}$ (max.)	P_{OUT}*	
		230 VAC	85 VAC to 265 VAC
LC5545LD	3.95 Ω	13 W	10 W
LC5546LD	1.9 Ω	20 W	16 W

* Based on the thermal ratings; the allowable maximum output powers can be up to 120% to 140% of the rated values. However, the maximum output powers may be limited in an application with a low output voltage or according to a maximum duty cycle for designing a transformer.

Applications

- LED Lighting Equipment
- LED Bulbs

Contents

1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified, T_A = 25 °C.

Parameter	Pin	Symbol	Conditions	Rating	Unit	Remarks
Drain Current	8–1	I_{DPEAK}	Single pulse	2.5	A	LC5545LD
				4.0		LC5546LD
Avalanche Energy	8–1	E_{AS}	Single pulse, V_{DD} = 99 V, L = 20 mH, I_{LPEAK} = 2.0 A	47	mJ	LC5545LD
			Single pulse, V_{DD} = 99 V, L = 20 mH, I_{LPEAK} = 2.7 A	86		LC5546LD
VCC Pin Voltage	2–1	V_{CC}		35	V	
OCP Pin Voltage	3–1	V_{OCP}		−2.0 to 5.0	V	
FB Pin Voltage	4–1	V_{FB}		−0.3 to 7.0	V	
OVP Pin Voltage	6–1	V_{OVP}		−0.3 to 5.0	V	
Power MOSFET Power Dissipation	8–1	P_{D1}		0.97	W	When mounted on a board with a size of 15 mm × 15 mm
Operating Ambient Temperature	—	T_{OP}		−55 to 125	°C	
Storage Temperature	—	T_{stg}		−55 to 125	°C	
Channel Temperature	—	T_{ch}		150	°C	

2. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

2.1. Electrical Characteristics of Control Parts

Unless specifically noted, T_A = 25 °C, V_{CC} = 20 V.

Parameter	Pin	Symbol	Min.	Typ.	Max.	Unit	Remarks
Power Supply Startup Operation							
Operation Start Voltage	2–1	$V_{CC(ON)}$	13.8	15.1	17.3	V	
Operation Stop Voltage[1]	2–1	$V_{CC(OFF)}$	8.4	9.4	10.7	V	
Circuit Current in Operation	2–1	$I_{CC(ON)}$	—	—	4.7	mA	
Startup Circuit Operation Voltage	8–1	$V_{STARTUP}$	18	21	24	V	
Startup Current	2–1	$I_{CC(STARTUP)}$	−8.5	−4.0	−1.5	mA	V_{CC} = 13 V
Startup Current Biasing Threshold Voltage[1]	2–1	$V_{CC(BIAS)}$	9.5	11.0	12.5	V	
Normal Operation							
PWM Operation Frequency	8–1	f_{OSC}	60	72	84	kHz	LC5545LD
			50	60	70		LC5546LD
Maximum On-time	8–1	$t_{ON(MAX)}$	8.0	9.3	11.2	µs	LC5545LD
			9.0	11.2	13.4		LC5546LD
FB Pin Control Minimum Voltage	4–1	$V_{FB(MIN)}$	0.50	0.85	1.20	V	
Maximum Feedback Current	4–1	$I_{FB(MAX)}$	−40	−25	−10	µA	
Leading Edge Blanking Time	3–1	$t_{ON(LEB)}$	—	600	—	ns	
Quasi-resonant Operation Threshold Voltage 1	3–1	$V_{BD(TH1)}$	0.14	0.24	0.34	V	
Quasi-resonant Operation Threshold Voltage 2	3–1	$V_{BD(TH2)}$	0.11	0.16	0.21	V	
Protection Function							
Overcurrent Detection Threshold Voltage	3–1	V_{OCP}	−0.66	−0.60	−0.54	V	
OCP Pin Source Current	3–1	I_{OCP}	−120	−40	−10	µA	
OCP Pin OVP Threshold Voltage	3–1	$V_{BD(OVP)}$	2.2	2.6	3.0	V	
OLP Threshold Voltage	4–1	$V_{FB(OLP)}$	4.1	4.5	4.9	V	
OVP Pin OVP Threshold Voltage	6–1	$V_{OVP(OVP)}$	1.6	2.0	2.4	V	
VCC Pin OVP Threshold Voltage	2–1	$V_{CC(OVP)}$	28.5	31.5	34.0	V	
Thermal Shutdown Operating Temperature	—	$T_{J(TSD)}$	135	—	—	°C	

[1] Always in the condition of $V_{CC(BIAS)} > V_{CC(OFF)}$.

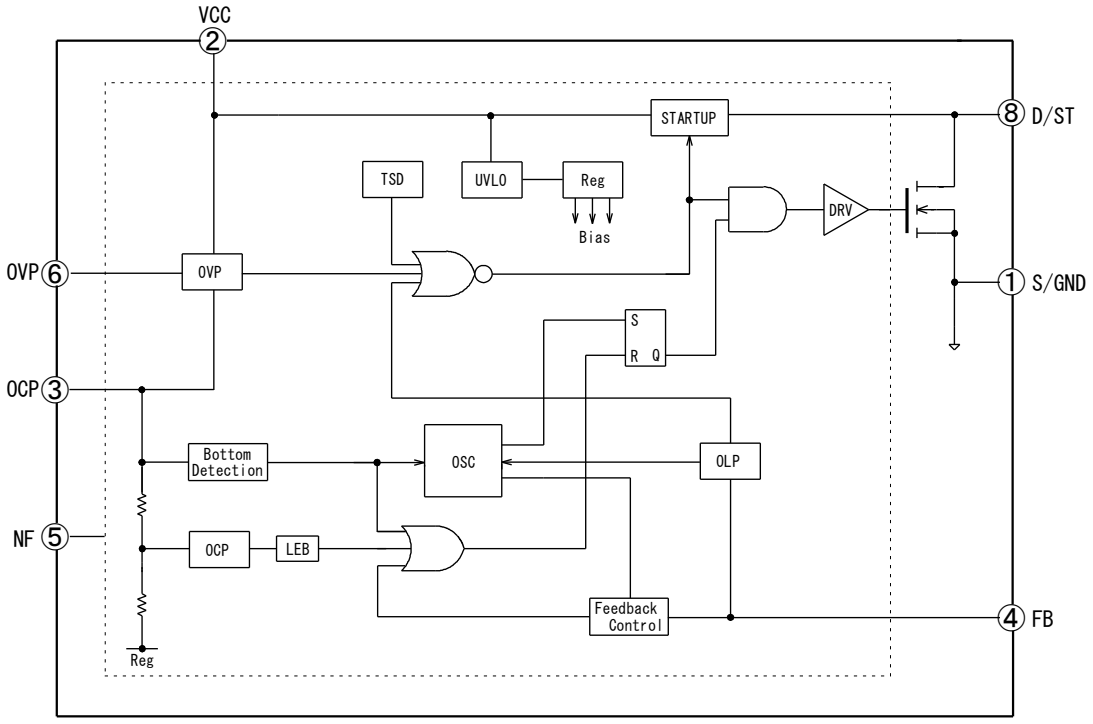
2.2. Electrical Characteristics of Power MOSFET

Unless otherwise specified, T_A = 25 °C.

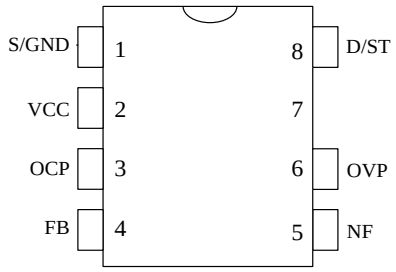
Parameter	Pin	Symbol	Min.	Typ.	Max.	Unit	Remarks
Drain-to-Source Breakdown Voltage	8 – 1	V_{DSS}	650	—	—	V	LC5545LD LC5546LD
Drain Leakage Current	8 – 1	I_{DSS}	—	—	300	μA	
On-resistance	8 – 1	$R_{DS(ON)}$	—	—	3.95	Ω	LC5545LD
			—	—	1.9		LC5546LD
Switching Time	8 – 1	t_f	—	—	250	ns	LC5545LD
			—	—	400		LC5546LD
Thermal Resistance(1)	—	θ_{ch-c}	—	—	42	°C/W	LC5545LD
			—	—	35.5		LC5546LD

(1) Refers to the thermal resistance between the channel of the power MOSFET and the case. The case temperature, T_C, is measured at the center of the branding side on the case.

3. Block Diagram



4. Pin Configuration Definitions



Pin Number	Pin Name	Description
1	S/GND	Power MOSFET source and control ground
2	VCC	Power supply voltage input for control part and OCP pin overvoltage protection signal input
3	OCP	Overcurrent protection signal input, quasi-resonant signal input, and overvoltage protection signal input
4	FB	Feedback signal input and overload protection signal input
5	NF	(No function assigned)(1)
6	OVP	OVP pin overvoltage protection signal input
7	—	(Pin removed)
8	D/ST	Power MOSFET drain and startup current input

(1) Should be connected to the S/GND pin (pin 1) with a minimum-length trace for stable operations.

5. Typical Application

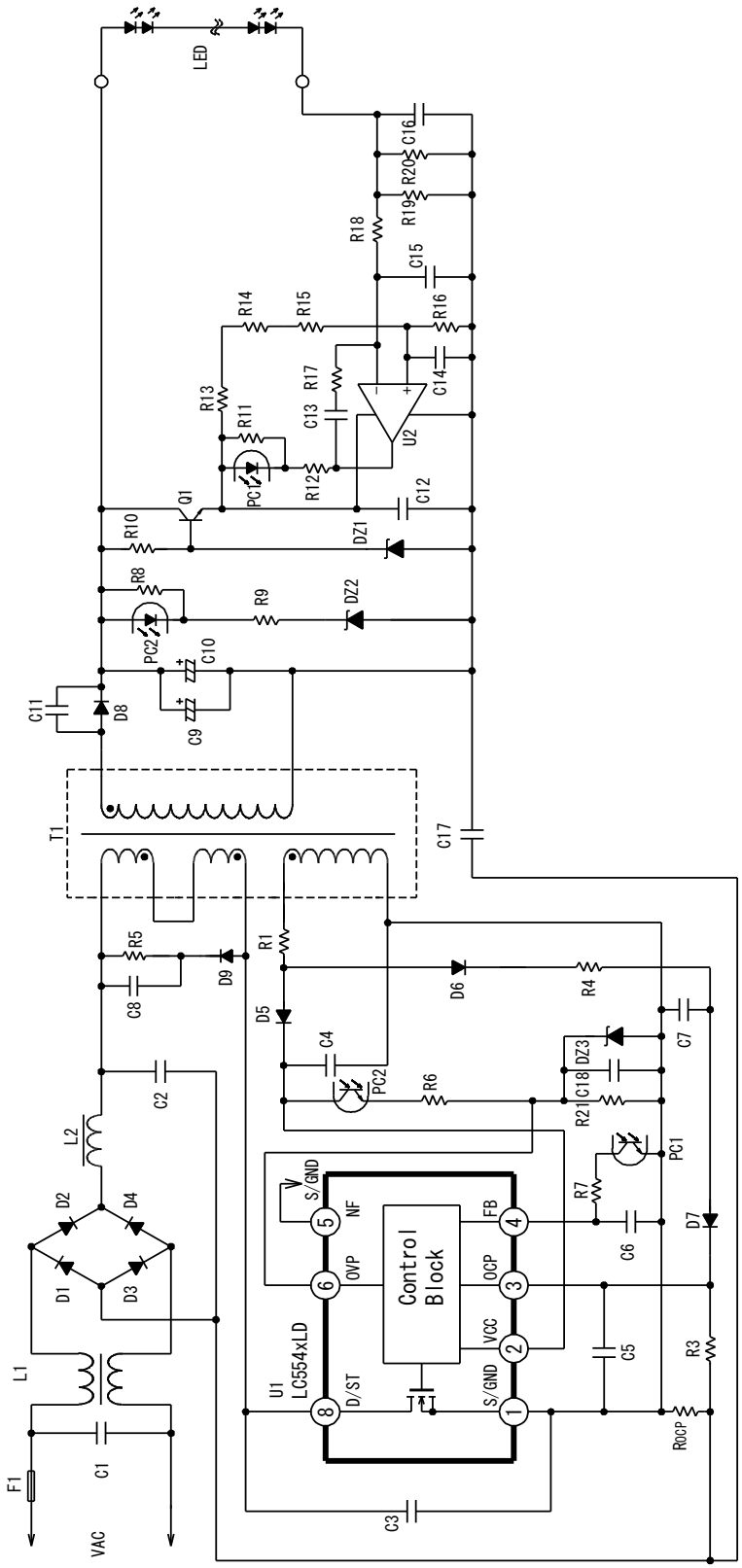


Figure 5-1. Typical Application

6. Physical Dimensions

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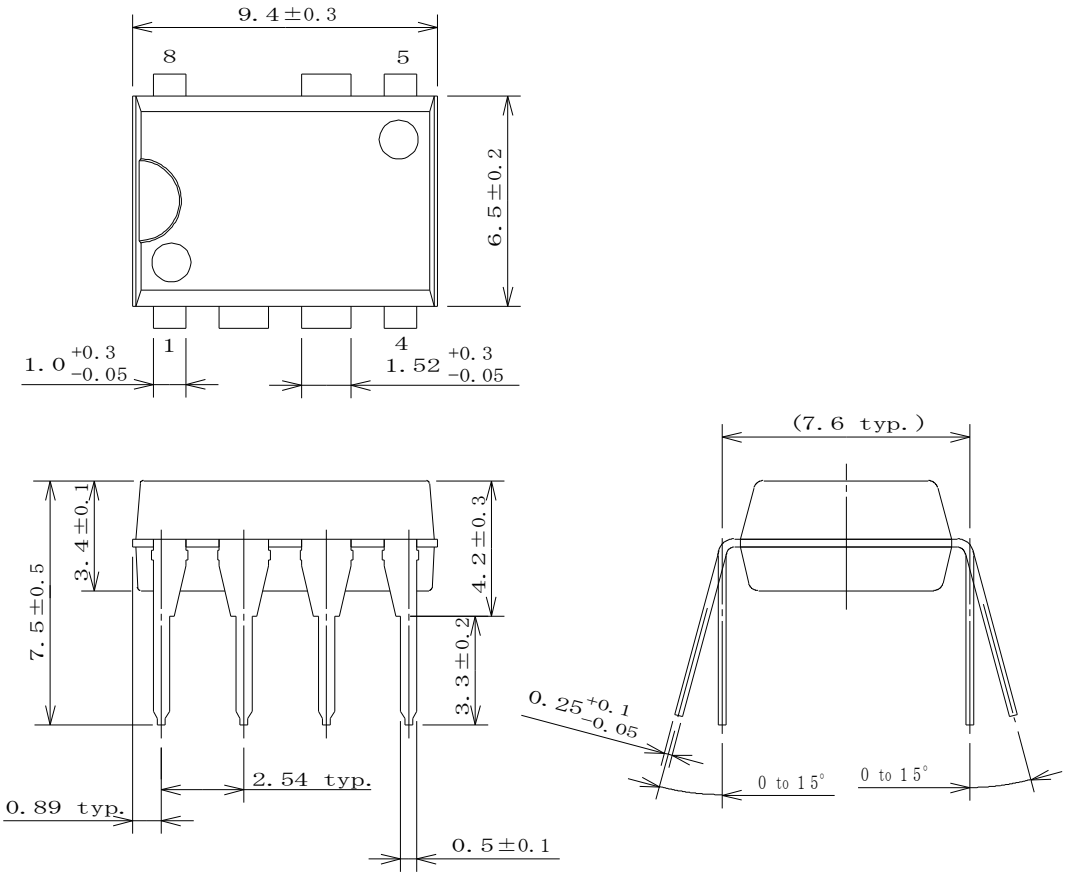
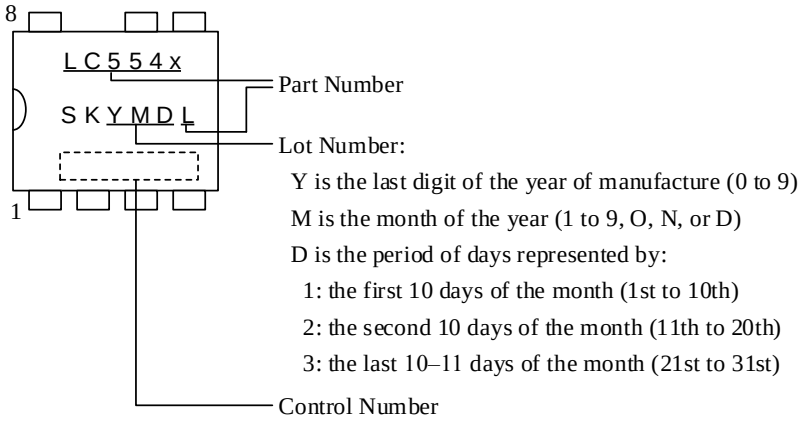


NOTES:

- Dimensions in millimeters
- Pb-free (RoHS compliant)

7. Marking Diagram



8. Operational Description

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−). All the characteristic values given in this section are typical values, unless they are specified as minimum or maximum.

8.1. Startup Operation

8.1.1. Startup Time

Figure 8-1 shows the VCC pin peripheral circuit. The IC has the startup circuit connected to the D/ST pin. When the D/ST pin voltage reaches the Startup Circuit Operation Voltage, $V_{STARTUP}$ = 21 V, the startup circuit starts to operate. During the startup process, the constant current, $I_{CC(STARTUP)}$ = −4.0 mA, charges C4 connected to the VCC pin. When the VCC pin voltage increases to $V_{CC(ON)}$ = 15.1 V, the IC starts to operate. After that, the startup circuit is automatically cut off to eliminate power dissipation by the startup circuit.

The startup time is determined by the capacitor C4. Use a ceramic or film capacitor for C4, and set its value to 0.22 µF to 22 µF when a general power supply specification is to be applied. The approximate value of the startup time can be calculated by the following equation:

$$t_{START} \fallingdotseq C4 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{\left|I_{CC(STARTUP)}\right|}. \quad (1)$$

Where:

t_{START} is the startup time (s), and
$V_{CC(INT)}$ is the initial VCC pin voltage (V).

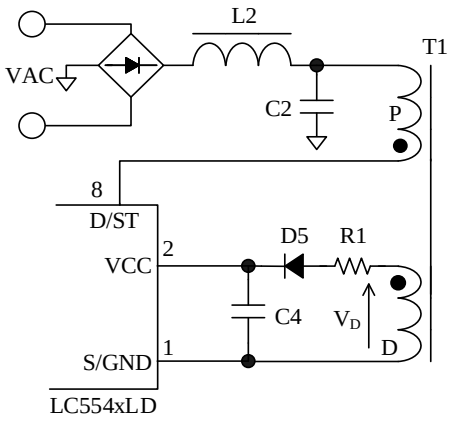


Figure 8-1. VCC Pin Peripheral Circuit

8.1.2. Undervoltage Lockout (UVLO)

Figure 8-2 shows the relationship of the VCC pin voltage and the circuit current, I_{CC}. When the VCC pin voltage reaches the Operation Start Voltage, $V_{CC(ON)}$ = 15.1 V, the control circuit starts to operate, then the circuit current increases. When the VCC pin voltage decreases to $V_{CC(OFF)}$ = 9.4 V, the control circuit operation is stopped by the undervoltage lockout (UVLO) circuit, and is put back to the state before startup. After the IC starts switching operation, the rectified auxiliary winding voltage is supplied to the VCC pin. The auxiliary winding voltage, V_D, is presented in Figure 8-1. In the variation range of the input and output specifications, the winding turns of the auxiliary winding, D, should be adjusted so that the VCC pin voltage falls within the range defined by Equation (2). The reference voltage across an auxiliary winding is about 20 V.

$$V_{CC(BIAS)MAX} < V_{CC} < V_{CC(OVP)MIN},$$

$$\text{that is, } 12.5\ \text{V} < V_{CC} < 28.5\ \text{V}. \quad (2)$$

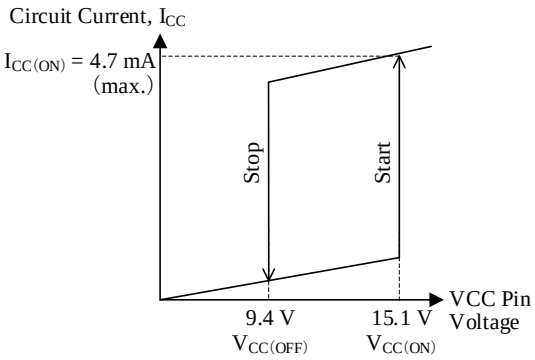


Figure 8-2. VCC Pin Voltage vs. Circuit Current, I_{CC}

8.1.3. Bias Assist Function

Figure 8-3 shows a VCC pin voltage behavior during the startup period. When the VCC pin voltage decreases to the Startup Current Biasing Threshold Voltage, $V_{CC(BIAS)}$ = 11.0 V, the bias assist function is activated. While the bias assist function is operating, the VCC pin voltage is kept almost constant because a decrease in the VCC pin voltage is regulated by a startup current from the startup circuit. While the output voltage rises, the VCC pin voltage increases to the target voltage with the slope determined by the voltage drop caused by increasing IC current and the voltage rise across the auxiliary winding, V_D, which is proportional to the output voltage.

The bias assist function reduces C4 capacitance. In addition, the response time of the OVP function can be shortened because the VCC pin voltage rise along with the output voltage rise also becomes faster. To avoid a startup failure, be sure to check the startup operation based on operations in an actual application, and to adjust a circuit

constant including C4.

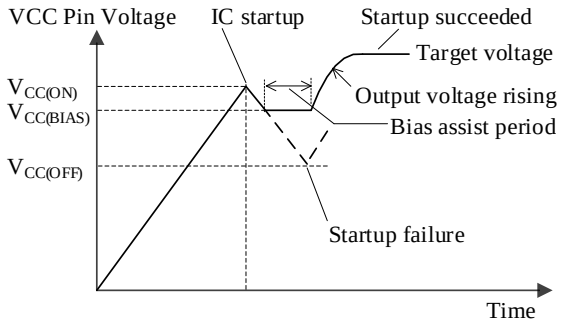


Figure 8-3. VCC Pin Voltage at Startup

8.1.4. Auxiliary Winding

In actual operation of power supply circuits, the transient surge voltage that occurs at power MOSFET turn-off induces a voltage across the auxiliary winding, D. C4 is charged at the peak of the induced voltage. The surge voltage increases as the output current, I_{OUT} increases. Thus, the VCC pin voltage increases as I_{OUT} increases, as shown in Figure 8-4. When the VCC pin voltage increases to $V_{CC(OVP)}$ = 31.5 V or more, the VCC pin overvoltage protection (VCC_OVP) is activated. To prevent the C4 peak charging, add R1 with a value ranging from several ohms to several ten ohms, in series with D5 (see Figure 8-5). The optimal value of R1 should be determined with a transformer set for an actual application, because the variation of the VCC pin voltage depends on the transformer's structural design.

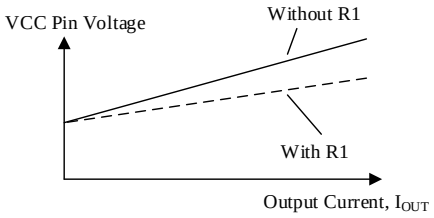


Figure 8-4. I_{OUT} vs. VCC with or without R1

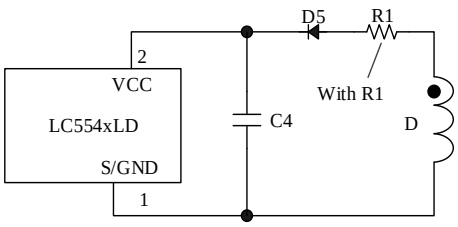


Figure 8-5. VCC Pin Peripheral Circuit to Reduce Effect of Output Current

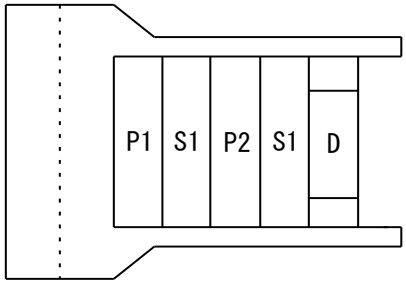
In the following cases, the VCC pin voltage is more susceptible to the effect of I_{OUT}. Care must be taken in the placement of the auxiliary winding, D, when designing your transformer.

- When poor coupling between the primary and secondary windings causes high surge voltage in the conditions such as low output voltage and high output current.
- When poor coupling between the auxiliary winding, D, and the secondary winding causes the auxiliary winding voltage to be susceptible to the effect of surge voltage variation.

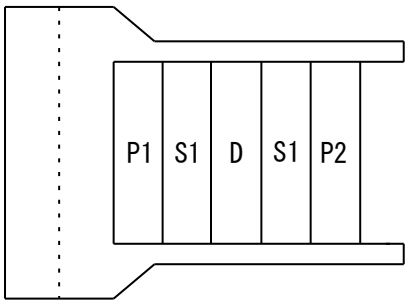
Figure 8-6 shows two transformer design examples for minimizing the impact of VCC surge voltage, with consideration given to the placement of the auxiliary winding, D (in which triple insulation wires are used for the primary or secondary winding, but no margin tapes used).

- **Winding Structural Example (a):**
  Separate the auxiliary winding, D, from the primary windings, P1 and P2 (P1 and P2 are two separated primary windings).

- **Winding Structural Example (b):**
  Improve the coupling between the secondary winding, S1, and the auxiliary winding, D.



Winding Structural Example (a)



Winding Structural Example (b)

Where:
P1 and P2 are the primary windings,
S1 is the secondary winding, and
D is the auxiliary winding.

Figure 8-6. Winding Structural Examples

8.1.5. Soft Start Function

Figure 8-7 shows the operation waveforms during the startup. The soft start function reduces the voltage and current stress of the power MOSFET and the secondary rectifier diode during the startup period. When the FB pin voltage reaches $V_{FB(MIN)}$ = 0.85 V, the IC shifts into the soft start operation. The soft start operation continues until the output current becomes constant, as shown in Figure 8-7. During the soft start operation, the output power gradually increases. To avoid a startup failure, be sure to check waveforms during the soft start operation and to adjust the power supply circuit so that the IC starts with the following conditions.

- The VCC pin voltage maintains over the Operation Stop Voltage, $V_{CC\ (OFF)}$.
- The output current reaches the target value before the overload protection (OLP) is activated (i.e., the FB pin voltage is less than $V_{FB(OLP)}$ = 4.5 V).

8.1.6. Operation Mode at Startup

Figure 8-7 shows the operation mode during the startup.

After the startup, when the FB pin voltage reaches $V_{FB(MIN)}$ = 0.85 V, the IC starts a PWM switching operation. The LC5540LD series requires different PWM operation frequencies, f_{OSC}, as follows: 72 kHz for the LC5545LD, and 60 kHz for the LC5546LD.

When the auxiliary winding voltage rises along with the output voltage, the positive voltage on the OCP pin also rises. When the OCP pin voltage reaches $V_{BD(TH1)}$ = 0.24 V or more, the IC shifts into the quasi-resonant operation.

Figure 8-8 shows the OCP pin voltage waveforms on an expanded time scale when the IC shifts into quasi-resonant operation mode from PWM operation (point A in Figure 8-7).

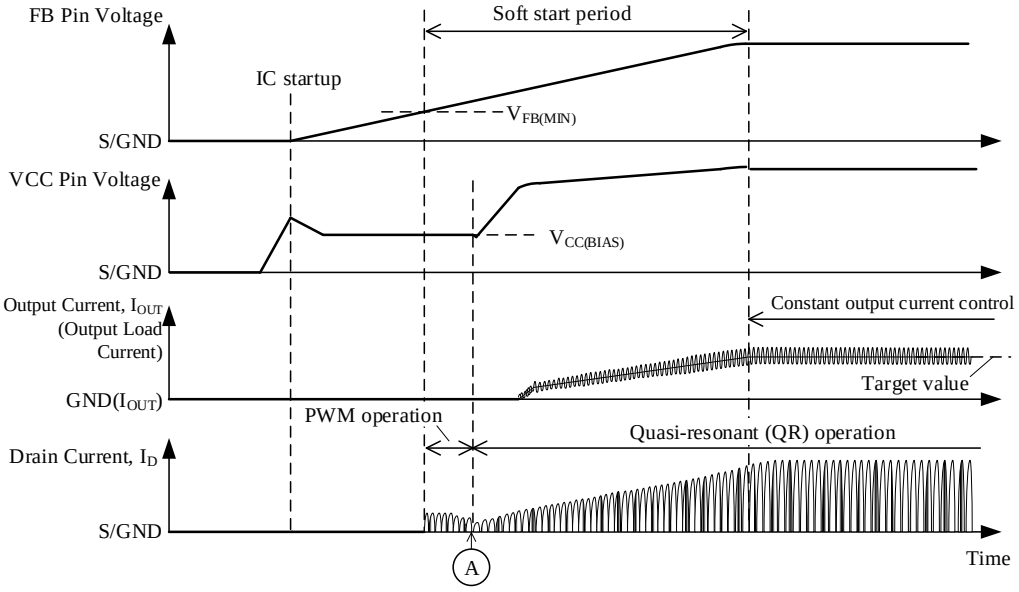


Figure 8-7. Soft Start Operation Waveforms at Startup

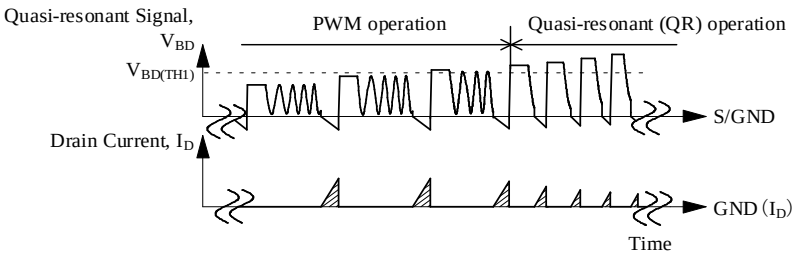


Figure 8-8. OCP Pin Voltage Waveforms on Expanded Time Scale (Point A)

8.2. On-time Control Operation

Figure 8-9 shows the peripheral circuit of the FB pin, whereas Figure 8-10 shows the on-time control. The IC controls an output current with the voltage mode, which controls an on-time depending on an output load, and the average current control. In the average current control shown in Figure 8-10, the IC compares the voltage drop of the secondary-side constant current detection resistor with the reference voltage by the secondary operational amplifier. Then, the output of the secondary operational amplifier is run through the optocoupler PC1 to the FB pin, and its output is averaged at the FB pin. The IC compares the averaged voltage at the FB pin with the internal oscillator (OSC) output by the internal FB comparator to control the on-time. The OSC indicates the oscillator circuit to control operations such as the PWM operation frequency, the quasi-resonant oscillation, and the maximum on-time limit.

The recommended value of capacitor, C6, connected to the FB pin is approximately 2.2 μF.

The IC controls the constant output current according to loads as follows:

- **When the output current becomes less than the target value**

When the output current decreases to less than the target value, the power supply circuit operates as follows: The voltage drop across the resistor that is for constant current detection in the secondary side becomes low. Therefore, the current through the optocoupler decreases. This leads to a decrease in the primary-side feedback current. Thus, the averaged FB pin voltage and on-time increase, and the output current increases.

- **When the output current becomes greater than the target value**

When the output current increases to greater than the target value, the power supply circuit operates opposite to the above as follows: The voltage drop across the resistor that is for constant current detection in the secondary side becomes high. Therefore, the current through the optocoupler increases. This leads to an increase in the primary-side feedback current. Thus, the averaged FB pin voltage and on-time decrease, and the output current decreases.

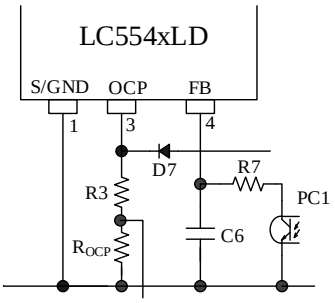


Figure 8-9. FB Pin Peripheral Circuit

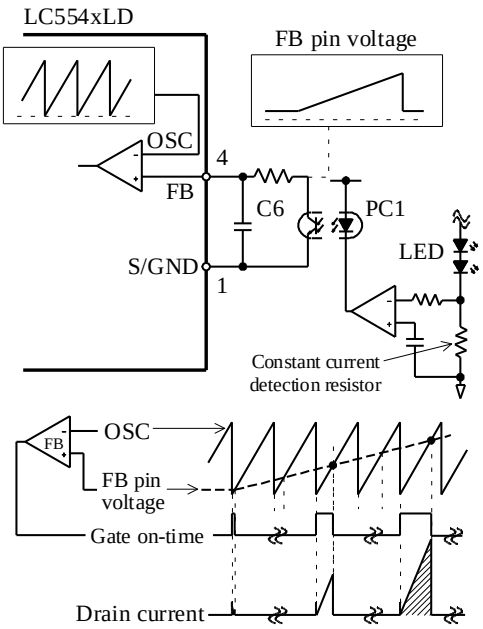


Figure 8-10. On-time Control

Figure 8-11 shows the average input current waveform. The averaged FB pin voltage becomes constant. Since duty cycle is controlled according to the V_{IN} voltage (C2 voltage in Figure 5-1), an averaged input current becomes a sine waveform. This yields a high power factor.

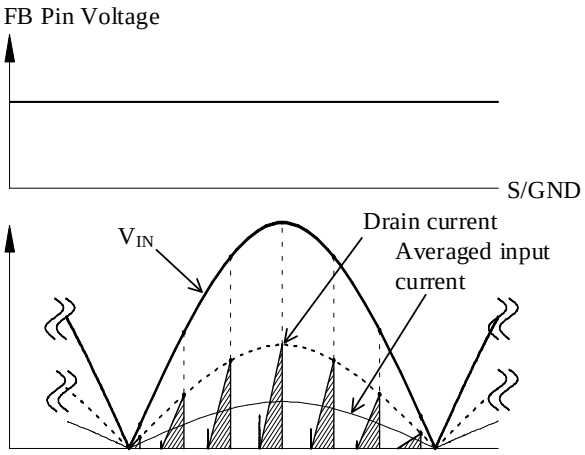


Figure 8-11. Averaged Input Current Waveform

8.3. Quasi-resonant Operation and Bottom-on Timing

8.3.1. Quasi-resonant Operation

Figure 8-12 shows the circuit of a flyback converter. The flyback converter is a system which transfers the energy stored in the transformer to the secondary side when the primary-side power MOSFET is turned off. The MOSFET stays in the off state even after the energy is completely transferred to the secondary side. During the off state, the voltage between the drain and source, V_{DS}, begins free oscillation based on the primary inductance, L_P, and the capacitance between the drain and source, C_V. The quasi-resonant operation provides V_{DS} bottom-on operation that the power MOSFET turns on at the lowest voltage point of V_{DS} free oscillation. Figure 8-13 shows an ideal V_{DS} waveform during the bottom-on operation. The bottom-on operation reduces switching loss and switching noise. This results in a power supply with high efficiency and low noise.

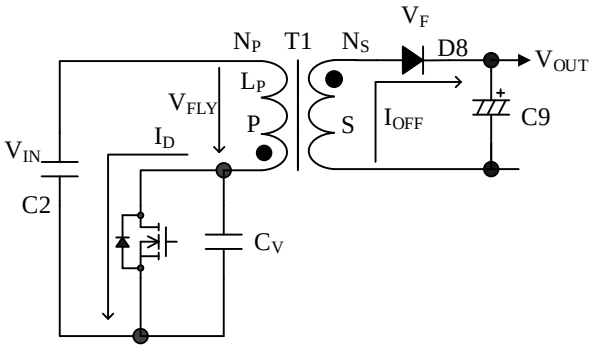


Figure 8-12. Basic Flyback Converter Circuit

The symbols in Figure 8-12 represent as follows:
V_{IN} is the input voltage,
V_{FLY} is the flyback voltage calculated by

$$V_{FLY} = \frac{N_P}{N_S} \times (V_{OUT} + V_F),$$

N_P is the number of turns in the primary winding,
N_S is the number of turns in the secondary winding,
V_{OUT} is the output voltage,
V_F is the forward voltage drop of the secondary rectifier diode,
I_D is the drain current of the power MOSFET,
I_{OFF} is the current running through the secondary rectifier diode during the power MOSFET off-period,
C_V is the voltage resonant capacitor, and
L_P is the primary inductance.

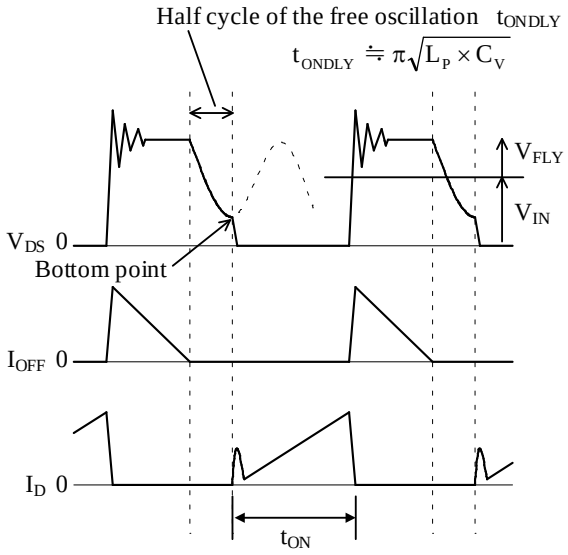


Figure 8-13. Ideal Bottom-on Operation Waveforms (Power MOSFET Turns On at the Lowest Voltage of V_{DS} Waveform)

8.3.2. Bottom-on Timing Setup

Figure 8-14 shows an OCP pin peripheral circuit, Figure 8-15 shows the waveform of an auxiliary winding voltage. The OCP pin detects the auxiliary winding voltage, which is synchronized with the V_{DS} waveform, through a delay circuit (D6, R4, C7, and D7 in Figure 8-14). The bottom-on operation is controlled by the delayed signal. The delay time, t_{ONDLY}, is the period from when V_{DS} free oscillation starts to when the power MOSFET turns on. The delay time is then adjusted by the delay circuit. During the power MOSFET turn-off, the positive voltage is supplied through the delay circuit to the OCP pin from auxiliary winding. This input signal to the OCP pin is defined as a quasi-resonant signal, V_{BD}.

When the V_{BD} increases to the Quasi-resonant Operation Threshold Voltage 1 ($V_{BD(TH1)}$ = 0.24 V) or more after the power MOSFET turns off, the IC maintains the power MOSFET in an off state. After that, when the V_{BD} decreases to the Quasi-resonant Operation Threshold Voltage 2 ($V_{BD(TH2)}$ = 0.16 V) or less, the IC turns on the power MOSFET and automatically raise the threshold voltage to $V_{BD(TH1)}$ to prevent malfunctions caused by the noise added to the OCP pin.

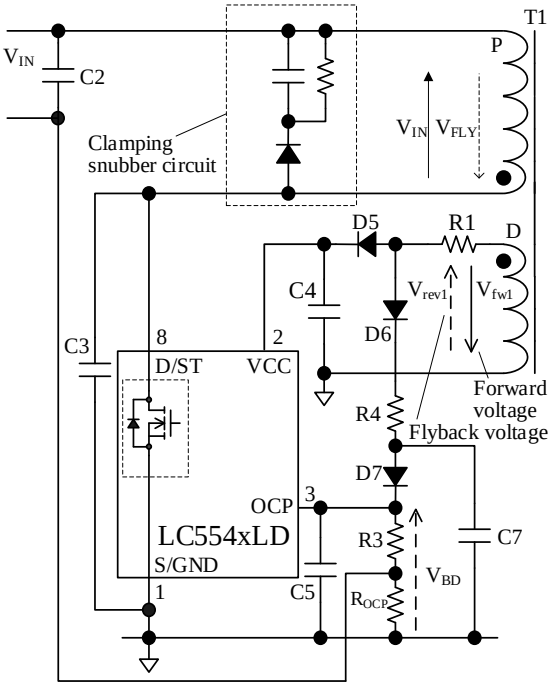


Figure 8-14. OCP Pin Peripheral Circuit

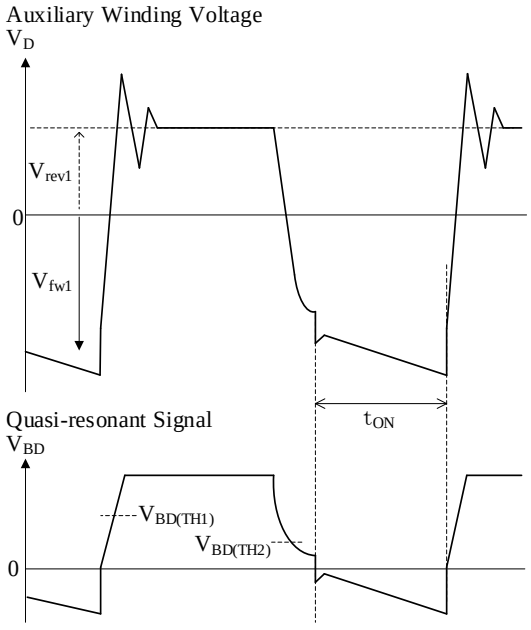


Figure 8-15. Auxiliary Winding Voltage

The delay time, t_{ONDLY} is determined by the constant values of the delay circuit. The values should be adjusted so that the power MOSFET turns on at the bottom of the V_{DS} waveform. The peak voltage of the quasi-resonant signal, $V_{BD(PK)}$, and the effective pulse width of the quasi-resonant signal, t_{QR}, should be adjusted as follows with the variations of R3 and R4 taken into account: $V_{BD(PK)}$ = 1.5 V to 2.0 V, and $t_{QR} \geq 1.2$ µs. These conditions must be fulfilled within the power supply input and output ranges (see Figure 8-16).

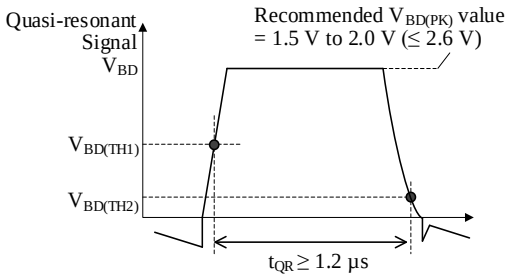


Figure 8-16. The Effective Pulse Width of Quasi-Resonant Signal

R3, R4, C5, and C7 should be set as follows:

- **R3**
  100 Ω to 330 Ω (reference value)

- **R4**
  R4 should be adjusted so that $V_{BD(PK)}$ meets the following conditions:

- $V_{BD(PK)} \geq V_{BD(TH1)}$ under the lowest VCC pin voltage condition in the ranges of the input and output specifications.
- $V_{BD(PK)} < 2.6$ V under the highest VCC pin voltage condition in normal operation. 2.6 V is the OCP Pin OVP Threshold Voltage, $V_{BD(OVP)}$.

Because R_{OCP} is much less than R3, R4 is calculated as follows:

$$R4 = \frac{(V_{CC} - V_{BD(PK)} - 2 \times V_F) \times R3}{V_{BD(PK)}}. \quad (3)$$

For example, if the VCC = 16 V, R3 = 220 Ω, $V_{BD(PK)}$ = 1.5 V, and the forward voltage drop (V_F) of D6 and D7 = 0.8 V, R4 is approximately 1.89 kΩ. Hence, R4 is 1.8 kΩ in the E12 series.

If $t_{QR} < 1.2$ µs, t_{QR} should be set to 1.2 µs or more through the following adjustments:

- To raise $V_{BD(PK)}$, increase the R3value.
- To raise $V_{BD(PK)}$, reduce the R4 value.
- To increase the free oscillation period, increase the capacitance of the voltage resonant capacitor, C3. (The greater the C3 value, the higher the switching loss; therefore, be sure to check that the IC temperature ranges within the absolute maximum rating when increasing the C3 value.)

● **C5**
100 pF to 470 pF (reference value)

● **C7**

The delay time, t_{ONDLY}, is adjusted by the value of C7. To set the ideal bottom-on of V_{DS} (see Figure 8-13), adjust C7 value with measuring actual waveforms under the maximum AC input voltage and the maximum output power. Measurement waveforms are the power MOSFET drain voltage, V_{DS}, the quasi-resonant signal, V_{BD}, and the drain current, I_D. A measurement point is the maximum amplitude of V_{DS} waveform, $V_{DS(PEAK)}$. An initial constant for C7 is about 1000 pF.

- When the power MOSFET turn-on is earlier than the V_{DS} bottom point at the $V_{DS(PEAK)}$ as Figure 8-17 (A): Confirm the V_{DS} bottom point at the initial constant, and then increase the value of C7 gradually until the power MOSFET turn-on point matches the V_{DS} bottom point.
- When the power MOSFET turn-on is later than the V_{DS} bottom point at the $V_{DS(PEAK)}$ as Figure 8-17 (B): Confirm the V_{DS} bottom point at the initial constant, and then increase the value of C7 gradually until the power MOSFET turn-on point matches the V_{DS} bottom point.

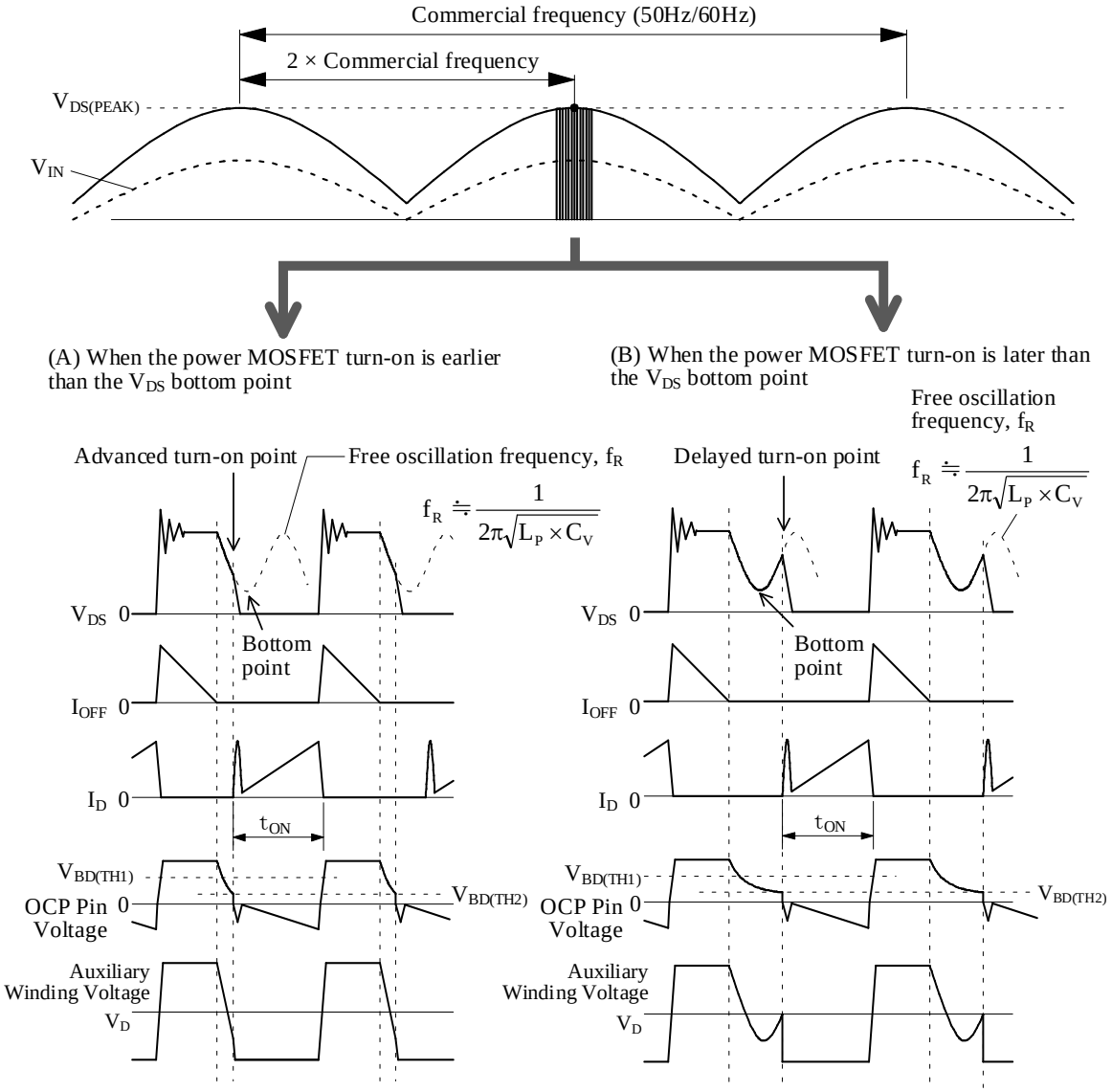


Figure 8-17. V_{DS} Waveforms at the $V_{DS(PEAK)}$

8.3.3. BD Blanking Time

Figure 8-18 shows the normal and inappropriate waveforms of the OCP pin voltage. An inappropriate operation is caused by poor coupling between the primary winding and the secondary winding of the transformer. A transformer with $N_P >> N_S$ (e.g., low output power design) has poor coupling and large leakage inductance. N_P and N_S indicate the number of turns of the primary winding and secondary winding, respectively. The poor coupling causes high surge voltage ringing at the OCP pin through the auxiliary winding when the power MOSFET turns off. The OCP pin has a blanking period of 250 ns (max.). In this period, the IC does not detect the OCP pin input signal (i.e., quasi-resonant signal). If the period when a surge voltage is being added to the OCP pin becomes longer than the blanking period, the power MOSFET can start switching at a high frequency because the IC responds to the surge. As a result, power dissipation in the internal power MOSFET increases. When the junction temperature reaches its absolute maximum rating, the power MOSFET can be damaged. When such high frequency operation occurs, the following adjustments are required:

- Add C5 of Figure 8-14 near the IC with minimizing a trace length between the OCP and S/GND pins.
- Redesign the PCB so that the trace of the OCP pin to the S/GND pin is separated from large current traces.
- Redesign the transform so that the coupling of the primary winding and the auxiliary winding is poor.
- Adjust the value of a clamping snubber circuit.

To measure any surge voltage waveform on the OCP pin correctly, connect a test probe as short as possible to the OCP pin and the S/GND pin.

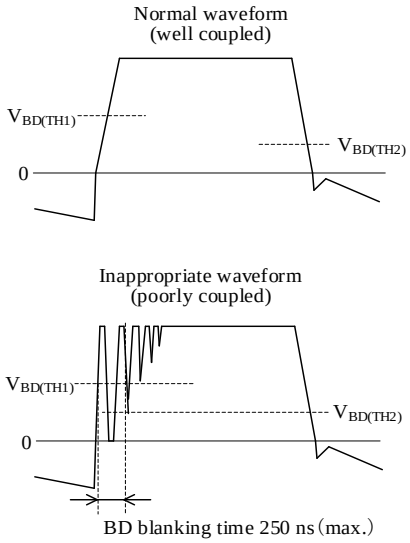


Figure 8-18. OCP Pin Voltage Waveforms Differed by Coupling Conditions of Transformer

8.4. Overvoltage Protection (OVP)

The IC has the overvoltage protection (OVP) for the VCC, OCP, and OVP pins. When these OVPs are activated, the IC stops switching operation in a latched state and the VCC pin voltage decreases. When it decreases to $V_{CC(BIAS)}$ = 11.0 V, the bias assist function is activated, and the startup current is supplied to the VCC pin. The VCC pin voltage then maintains at $V_{CC(OFF)}$ = 9.4 V or more, thus allowing the latched state to maintain.

To release the latched state, turn off the input voltage and decrease the VCC pin voltage below $V_{CC(OFF)}$.

8.4.1. VCC Pin Overvoltage Protection (VCC_OVP)

Figure 8-19 shows operational waveforms of the VCC pin overvoltage protection (VCC_OVP). When the voltage across the VCC and S/GND pins reaches $V_{CC(OVP)}$ = 31.5 V or more, the VCC_OVP is activated, and then the IC stops switching operation in a latched state. Because the VCC pin voltage is proportional to the output voltage, it can be used to detect an output overvoltage event such as an open load condition. The approximate secondary output voltage at VCC_OVP activation, $V_{OUT(OVP)}$, can be calculated by Equation (4) below:

$$V_{OUT(OVP)} = \frac{V_{OUT}}{V_{CC}} \times 31.5 \, . \qquad (4)$$

Where V_{OUT} is the secondary output voltage in normal operation, and V_{CC} is the VCC pin voltage in normal operation.

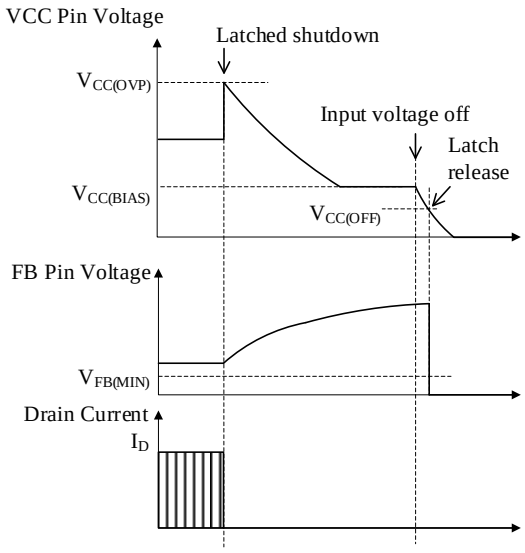


Figure 8-19. VCC_OVP Operational Waveforms

8.4.2. OCP Pin Overvoltage Protection (OCP_OVP)

Figure 8-20 shows operational waveforms of the OCP pin overvoltage protection (OCP_OVP). When the voltage across the OCP and S/GND pins reaches $V_{BD(OVP)}$ = 2.6 V or more, the OCP_OVP is activated. Then, the IC stops switching operation in a latched state. The OCP pin input voltage must be less than its rated maximum voltage of 5 V. The OCP pin overvoltage will occur due to improper settings, such as an improper setting of a quasi-resonant signal (V_{BD}), or a poor coupling of the transformer between the primary and secondary winding.

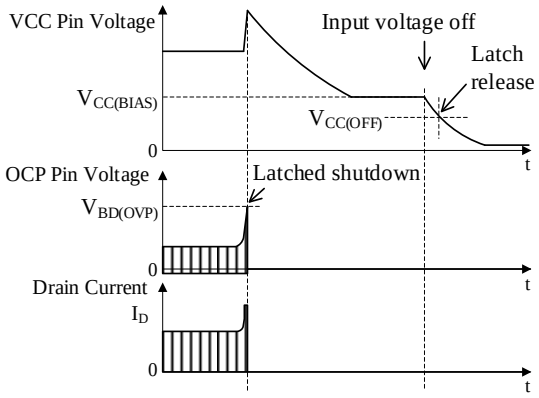


Figure 8-20. OCP_OVP Operational Waveforms

8.4.3. OVP Pin Overvoltage Protection (OVP_OVP)

Figure 8-21 shows operational waveforms of the OVP pin overvoltage protection (OVP_OVP). When the voltage across the OVP and S/GND pins reaches $V_{OVP(OVP)}$ = 2.0 V or more, the OVP_OVP is activated. Then, the IC stops switching operation in a latched state. The OVP pin input voltage must be less than its rated maximum voltage of 5 V. The OVP_OVP operates as the protection against abnormal conditions, such as a short-circuit load of serially connected LEDs. The IC detects the secondary output voltage through an optocoupler (PC2, as in Figure 5-1) and activates the OVP_OVP.

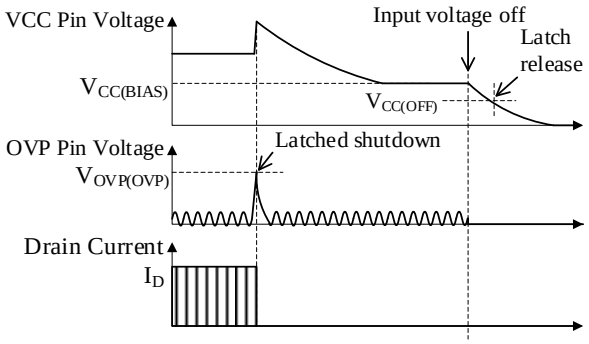


Figure 8-21. OVP_OVP Operational Waveforms

8.5. Overload Protection (OLP)

In the overload protection (OLP), the peak drain current is limited by the OCP operation. Figure 8-22 shows the FB pin peripheral circuit, whereas Figure 8-23 shows the OLP operational waveforms.

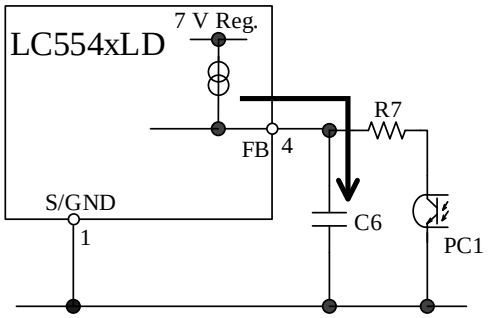


Figure 8-22. FB Pin Peripheral Circuit

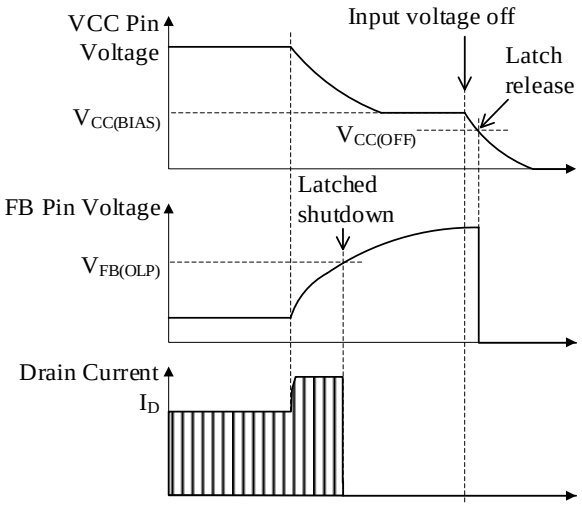


Figure 8-23. OLP Operational Waveforms

In the overload condition, the VCC pin voltage drops along with the output voltage drop. When the VCC pin voltage reaches the Startup Current Biasing Threshold Voltage, $V_{CC(BIAS)}$ = 11.0 V, the bias assist function is activated to suppress a reduction in the VCC pin voltage. Simultaneously, the output of the secondary-side error amplifier turns off as the output voltage decreases, then the optocoupler, PC1, is cut off. Since C6 connected to the FB pin is charged with the feedback current after the PC1 cutoff, the FB pin voltage increases. When the FB pin voltage reaches the OLP Threshold Voltage, $V_{FB(OLP)}$ = 4.5 V, the IC stops switching operation in a latched state (see Section 8.4).

To release the latched state, turn off the input voltage and decrease the VCC pin voltage below $V_{CC(OFF)}$.

The reference capacitance of C6 is about 1 µF to 4.7 µF. If the capacitance is too small, the OLP function may be activated when the IC restarts. C6 should be adjusted based on actual operations in your application.

8.6. Overcurrent Protection (OCP)

The overcurrent protection (OCP) detects the peak drain current of the power MOSFET on a pulse-by-pulse basis, and limits the output power.

8.6.1. OCP Detection Method and Leading Edge Blanking Function

The drain current of the power MOSFET is detected by the current detection resistor, R_{OCP}, placed between the OCP and S/GND pins, as shown in Figure 8-24. The detection signals, V_{ROCP}, are fed through R3 to the OCP pin.

The power MOSFET turns off when V_{ROCP} reaches the value obtained by Equation (5), below:

$$V_{ROCP} = -(|V_{OCP}| + R3 \times |I_{OCP}|) . \quad (5)$$

Where V_{OCP} is the overcurrent detection threshold voltage of −0.6 V, R3 is the value of R3, and I_{OCP} is the OCP pin source current of −40 µA.

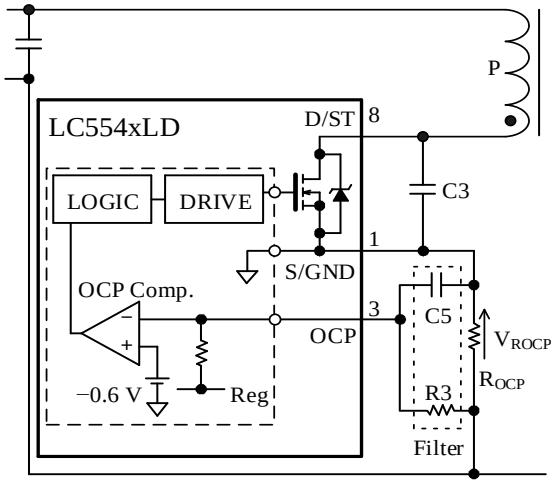


Figure 8-24. OCP Circuit for Negative Side Detect

To prevent malfunctions, connect a filter to the OCP pin. Set the constants of the filter (R3, C5) as follows:

- **R3**

To minimize the effects of a variation in the internal resistor, set R3 value to about 100 Ω to 330 Ω.

- **C5**

C5 value is about 100 pF to 470 pF. C5 must be a capacitor with good temperature characteristics. If the C5 value is too large, a response time of the OCP function may become slow. This causes the peak of drain current to be increased in transient conditions such as a startup.

The OCP function employs a peak current detection method. If the OCP pin detects a surge voltage at the power MOSFET turn-on edge, the power MOSFET may turn off. As a prevention against such operation, the IC has the Leading Edge Blanking Time ($t_{ON(LEB)}$ = 600 ns), which starts immediately after the power MOSFET turn-on.

When the power MOSFET turns on, the surge voltage width of the OCP pin voltage should be less than $t_{ON(LEB)}$, as shown in Figure 8-25. If the surge voltage width becomes $t_{ON\ (LEB)}$ or more, be sure to regulate the surge voltage value and surge voltage width by implementing the following settings:

- Adjust the timing of power MOSFET turn-on to the bottom point of V_{DS} waveform.
- Reduce the capacitance of the voltage resonant capacitor, C_V (i.e., C3).
- Reduce the capacitance of the secondary rectifier snubber capacitor.

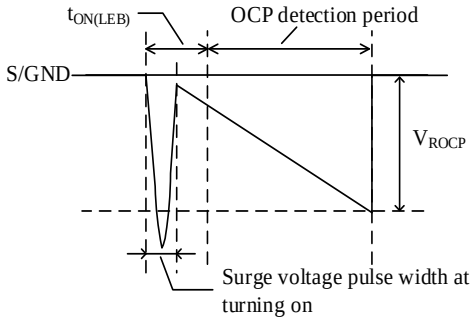


Figure 8-25. OCP Pin Voltage (Converted from Power MOSFET Drain Current by R_{OCP})

8.6.2. Input Compensation Function

The IC has the input compensation function that compensates the Overcurrent Detection Threshold Voltage, V_{OCP}, according to AC input voltages. In an application using a quasi-resonant converter with universal input (85 VAC to 265 VAC), the peak drain current of the power MOSFET decreases due to a higher operation frequency caused by an increased input voltage under a condition of constant output power.

Figure 8-26 shows the relationship between AC input voltage and the output current at OCP activation, $I_{OUT(OCP)}$, with the OCP input compensation function being activated or deactivated. When the IC without the input compensation, $I_{OUT(OCP)}$ increases as the AC input voltage increases (see "I_{OUT} without input compensation" in Figure 8-26). To regulate $I_{OUT(OCP)}$ at the maximum AC input voltage, add the OCP input compensation circuit (D_{X1}, DZ_{X1}, R_{X1}) as shown in Figure 8-27. The values of these components should be adjusted so that $I_{OUT(OCP)}$ at the maximum AC input voltage exceeds the target output current, I_{OUT} (see "I_{OUT} with appropriate input compensation" in Figure 8-26).

Figure 8-27 shows the OCP input compensation circuit, and Figure 8-28 shows the V_{fw1} and V_{fw2} voltages according to the AC input voltage. The compensation amount of V_{OCP} depends on values of the input compensation current, I, R_{X1}, R3, and R_{OCP}. The input compensation current, I, is calculated by the following equation:

$$I = \frac{V_{fw1} - V_{ZX1} - V_{FX1}}{R_{X1} + R3 + R_{OCP}}. \quad (6)$$

Where:
I is the input compensation current,
V_{fw1} is the forward voltage of the auxiliary winding, D proportional to input voltage,
V_{FX1} is the forward voltage of the rectifier diode D_{X1}, and
V_{ZX1} is the Zener voltage of the Zener diode DZ_{X1}.

The Overcurrent Detection Threshold Voltage, V_{ROCP}' applied with OCP input compensation is calculated by the following equation:

$$V'_{ROCP} = -(|V_{OCP}| + |R3 \times I_{OCP}| - R3 \times I). \quad (7)$$

Where:
I is the input compensation current,
R3 is the value of R3,
V_{OCP} is the overcurrent detection threshold voltage (−0.6 V), and
I_{OCP} is is OCP pin source current (−40 μA).

As the input voltage, V_{IN}, increases, the voltage drop across R3 by the input compensation current, I (i.e., R3 × I) increases. Then, the input compensation amount also increases, and the absolute value of V_{ROCP}' decreases.

The compensation start voltage of the OCP input voltage is determined by the Zener voltage (V_{ZX1}) of the Zener diode (DZ_{X1}). Set V_{ZX1} to the same voltage as V_{fw1} at the OCP input compensation starting point. The OCP pin voltage, including surge voltage, must be regulated within the rated voltages (−2.0 V to 5.0 V) under a condition of the maximum AC input voltage.

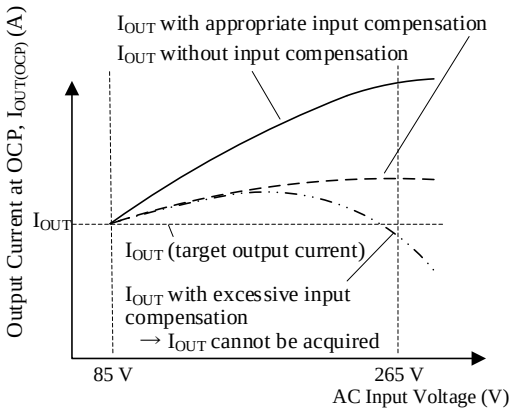


Figure 8-26. AC Input Voltage vs. Output Current at OCP (with or without OCP Input Compensation Function)

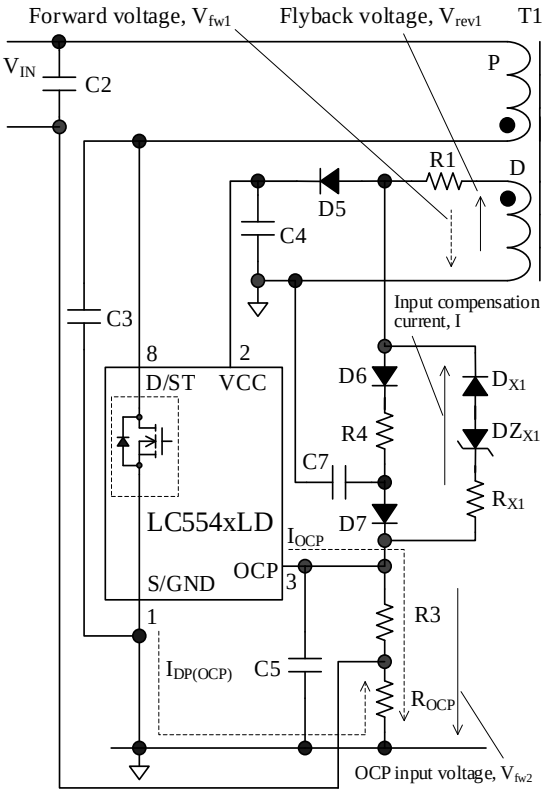


Figure 8-27. OCP Input Compensation Circuit

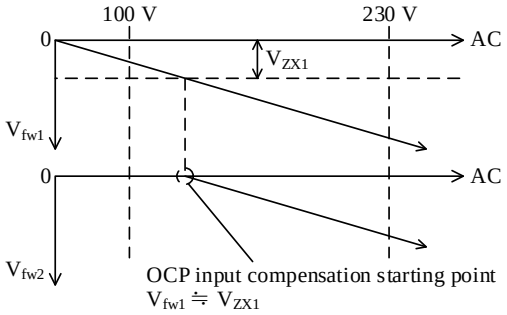


Figure 8-28. V_{fw1} and V_{fw2} vs. AC Input Voltages

8.6.3. OCP Threshold Voltage with or without Compensation Circuit

The overcurrent detection threshold voltage without an OCP input compensation circuit, V_{ROCP}, is calculated by Equation (8). When V_{ROCP} with reference to the S/GND pin becomes equal to the sum of V_{OCP} and the voltage across R3 (i.e., R3 × I_{OCP}), OCP is activated (see Figure 8-29).

$$V_{ROCP} = -\left|R_{OCP} \times I_{DP(OCP)}\right| = -(|V_{OCP}| + R3 \times |I_{OCP}|) . \quad (8)$$

Where:

V_{ROCP} is the overcurrent detection threshold voltage without an OCP input compensation circuit,
$I_{DP(OCP)}$ is the peak drain current during OCP operation,
V_{OCP} is the overcurrent detection threshold voltage (−0.6 V), and
I_{OCP} is the OCP pin source current (−40 µA).

The overcurrent detection threshold voltage with an OCP input compensation circuit, V_{ROCP}', is calculated by Equation (9).

When V_{ROCP}' with reference to the S/GND pin becomes equal to the sum of V_{OCP}, the voltage across R3 (i.e., R3 × I_{OCP}), and R3 × I, OCP is activated (see Figure 8-30).

$$V_{ROCP}' = -\left|R_{OCP} \times I_{DP(OCP)}'\right| = -(|V_{OCP}| + |R3 \times I_{OCP}| - R3 \times I) . \quad (9)$$

Where:

V_{ROCP}' is the overcurrent detection threshold voltage with an OCP input compensation circuit,
$I_{DP(OCP)}'$ is the peak drain current during OCP operation with OCP input compensation circuit,
V_{OCP} is the overcurrent detection threshold voltage (−0.6 V),
I_{OCP} is the OCP pin source current (−40 µA), and
I is the input compensation current.

Thus, the overcurrent detection threshold voltage will be changed by adding the OCP input compensation circuit for limiting the output power.

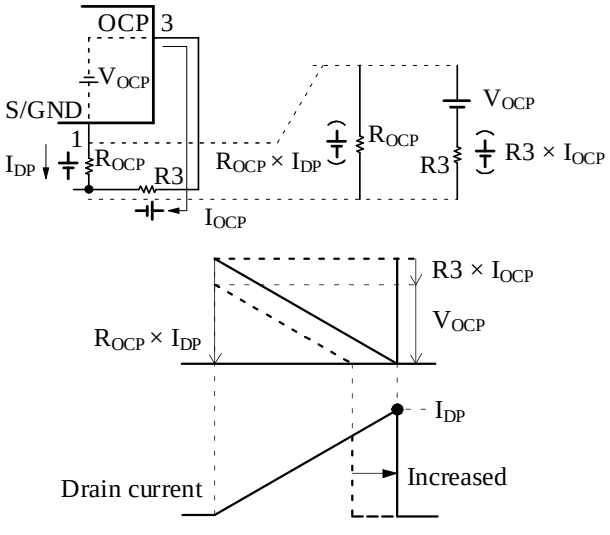


Figure 8-29. Without OCP Input Compensation Function

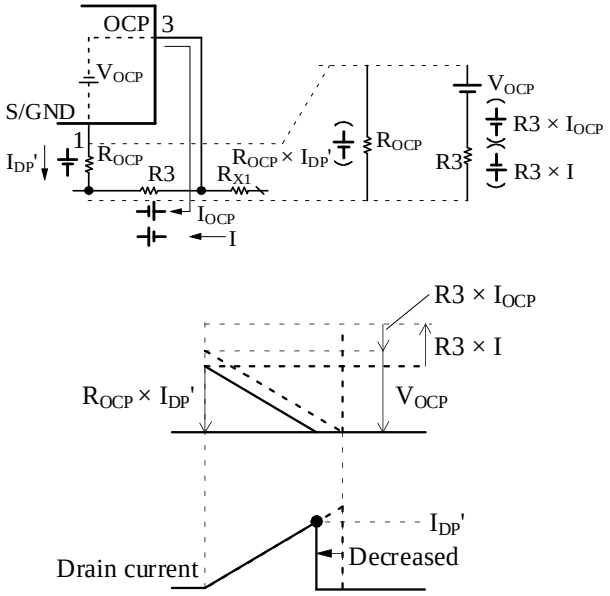


Figure 8-30. With OCP Input Compensation Function

8.6.4. Determining OCP Input Compensation Circuit Component Values

The component symbols used in this section are represented as follows:

I_{DP} is the peak drain current of the power MOSFET,
V_{FX1} is the forward voltage of the rectifier diode D_{X1},
V_{ZX1} is the Zener voltage of the Zener diode DZ_{X1},
V_{OCP} is the overcurrent detection threshold voltage (−0.6 V),
I_{OCP} is the OCP pin source current (−40 µA), and
I is the input compensation current.

For other component numbers, such as resistors, see Figure 8-27.

The peak drain current during OCP operation without OCP input compensation circuit, $I_{DP(OCP)}$, is expressed by Equation (10) obtained from Figure 8-29. $I_{DP(OCP)}$ is equal to the drain current limited by overcurrent detection threshold voltage without OCP input compensation in the minimum AC input voltage condition.

$$R_{OCP} \times \left|I_{DP(OCP)}\right| = |V_{OCP}| + R3 \times |I_{OCP}|$$
$$\therefore \left|I_{DP(OCP)}\right| = \frac{|V_{OCP}| + R3 \times |I_{OCP}|}{R_{OCP}}. \quad (10)$$

The peak drain current during OCP operation with OCP input compensation circuit, $I_{DP(OCP)}'$, is expressed by Equation (11) obtained from Figure 8-30:

$$R_{OCP} \times \left|I_{DP(OCP)}'\right| = |V_{OCP}| + R3 \times |I_{OCP}| - R3 \times I$$
$$\therefore \left|I_{DP(OCP)}'\right| = \frac{|V_{OCP}| + R3 \times (|I_{OCP}| - I)}{R_{OCP}}. \quad (11)$$

$I_{DP(OCP)}'$ in the maximum AC input voltage should be set to the peak drain current where the output current is equal to "I_{OUT} with appropriate input compensation" in Figure 8-26.

The input compensation current, I, can be expressed by the following equation obtained from Equations (10) and (11):

$$I = \left(\left|I_{DP(OCP)}\right| - \left|I_{DP(OCP)}'\right|\right) \times \frac{R_{OCP}}{R3}. \quad (12)$$

The forward voltage, V_{fw1}, at C2 peak voltage $V_{IN(PK)MAX}$ in the maximum AC input voltage is expressed as follows:

$$V_{fw1} = \frac{N_D \times V_{IN(PK)MAX}}{N_p}. \quad (13)$$

To supply input compensation current, I, in the maximum AC input voltage, calculate R_{X1} value as the following steps:

The input compensation current, I, can be expressed by the following equation:

$$I = \frac{V_{fw1} - V_{ZX1} - V_{FX1}}{R_{X1} + R3 + R_{OCP}}. \quad (14)$$

Assuming R3 << R_{X1} and R_{OCP} << R4, then:

$$R_{X1} = \frac{V_{fw1} - V_{ZX1} - V_{FX1}}{I}. \quad (15)$$

Substituting Equation (13) for Equation (15), R_{X1} is calculated as follows:

$$R_{X1} = \frac{\frac{N_D \times V_{IN(PK)MAX}}{N_p} - (V_{ZX1} + V_{FX1})}{I}. \quad (16)$$

8.6.5. Reference Design for OCP Input Compensation Circuit with Universal Input

A constant of the OCP input compensation circuit (DZ_{X1}, R_{X1}) that supports universal input specifications (85 VAC to 265 VAC) should be determined based on the actual performance in your application. Follow the procedures below when setting the constant:

1) Tentatively, set the OCP input compensation start voltage, $V_{IN(OCP\_ST)}$, to about 100 VAC to 130 VAC. In this reference design, $V_{IN(OCP\_ST)}$ = 120 VAC.
2) Set the circuit components to the following reference values.

Symbol	Reference Value	Remarks
$V_{IN(AC)}$	85 VAC to 265 VAC	AC input voltage
P_{OUT}	40 W	Output power
N_P	40 turns	Transformer primary winding turns
N_D	6 turns	Transformer auxiliary winding turns
R_{OCP}	0.2 Ω	OCP detection resistor
R3	220 Ω	OCP pin filter resistor
V_{FX1}	0.8 V	D_{X1} forward voltage drop

3) In the minimum AC input voltage (85 VAC) condition, measure the peak drain current during OCP operation, $I_{DP(OCP)}$.
4) In the maximum AC input voltage (265 VAC) condition, measure the drain current, $I_{DP(OCP)}'$, when the output current, $I_{OUT(OCP)}$, becomes the "I_{OUT} with appropriate input compensation" in Figure 8-26.
5) Calculate the constants of DZ_{X1} and R_{X1} from the circuit component constant 2) and the results of 3) and 4). Calculation examples are shown in below:

● **DZ_{X1}**

Calculate the forward voltage V_{fw1} of the auxiliary winding from Equation (13). If $V_{IN(OCP\_ST)}$ = 120 VAC, V_{fw1} is calculated as follows:

$$V_{fw1} = \frac{N_D}{N_p} \times V_{IN(PK)MAX} = \frac{N_D}{N_p} \times V_{IN(OCP\_ST)} \times \sqrt{2}$$

$$= \frac{6}{40} \times 120 \times \sqrt{2} = 25.5\ \text{V}.$$

Thus, select a Zener diode of Zener voltage V_{ZX1} = 27 V for DZ_{X1}.

● **R_{X1}**

If the results of 3) and 4) are $I_{DP(OCP)}$ = 3.0 A and $I_{DP(OCP)}'$ = 1.9 A, R_{X1} is calculated as follows:

First, calculate the input compensation current, I, from Equation (12).

$$I = \left(\left|I_{DP(OCP)}\right| - \left|I_{DP(OCP)}'\right|\right) \times \frac{R_{OCP}}{R3}$$

$$= (3.0 - 1.9) \times \frac{0.2}{220} = 1.0 \times 10^{-3}\ \text{A}.$$

Then, calculate R_{X1} from Equation (16).

$$R_{X1} = \frac{\frac{N_D \times V_{IN(PK)MAX}}{N_p} - (V_{ZX1} + V_{FX1})}{I}$$

$$= \frac{\frac{6 \times 265 \times \sqrt{2}}{40} - (27 + 0.8)}{1.0 \times 10^{-3}}$$

$$= 28.4 \times 10^3\ \Omega.$$

Thus, select R_{X1} = 27 kΩ of the E12 series.

6) Confirm that the output current during OCP operation, $I_{OUT(OCP)}$, is similar to "I_{OUT} with appropriate input compensation" in Figure 8-26, in an actual operation throughout AC input voltage ranges. If $I_{OUT(OCP)}$ is not appropriate, be sure to adjust the constants of DZ_{X1} and R_{X1} by changing the compensation startup voltage, $V_{IN(OCP\_ST)}$.

8.7. Thermal Shutdown (TSD)

When the junction temperature of the IC reaches the Thermal Shutdown Operating Temperature, $T_{J(TSD)}$ = 135 °C (min.), the thermal shutdown (TSD) is activated, and the IC stops switching operation in a latched state same as Section 8.4.

To release the latched state, turn off the input voltage and decrease the VCC pin voltage below $V_{CC(OFF)}$.

8.8. Maximum On-time Limitation Function

When the input voltage is low or in a transient state (e.g., at which the input voltage turns on or off), the IC limits the on-time of the internal power MOSFET to the Maximum On-time, $t_{ON(MAX)}$ (see Figure 8-31). $t_{ON(MAX)}$ is typically specified at 9.3 μs for the LC5545LD and at 11.2 μs for the LC5546LD, respectively. This reduces audible noise from the transformer and stress on the devices such as internal power MOSFET and secondary rectifier.

Be sure to ensure that the actual on-time is $<t_{ON(MAX)}$ in the minimum AC input voltage and the maximum load.

If your application uses a transformer, whose on-time is $\geq t_{ON(MAX)}$ under the condition of the minimum AC input voltage and the maximum load, the output power decreases due to the on-time of the power MOSFET limited to $t_{ON(MAX)}$ in the condition of the minimum AC input voltage. In this case, redesign the transformer so that the on-time becomes lower with following settings:

- Decrease the inductance of the transformer, L_P, to raise the switching frequency and reduce the on-time.
- Decrease the N_P/N_S, which is the turn ratio of the primary side and the secondary side to reduce the duty cycle.

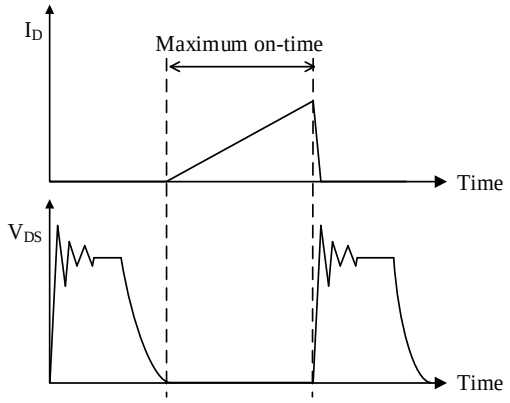


Figure 8-31. Maximum On-time Confirmation

9. Design Notes

9.1. External Components

The components fulfilled the use conditions should be used.

● **Output Smoothing Electrolytic Capacitor**

Apply proper design margin to ripple current, ripple voltage, and temperature rise. The electrolytic capacitor used must have high allowable ripple current for switching power supplies and low impedance.

● **Transformer**

Apply proper design margin to core temperature rise caused by core loss and copper loss. Because switching currents contain high frequency currents, a skin effect may become a consideration. For this reason, the wire diameter of a transformer winding should be selected by taking the RMS of the operating current into account, and the current density should be 3 A/mm^2 to 4 A/mm^2. If the measures to further reductions in temperature are still necessary, the following should be taken into account to increase the total surface area of the wiring:

- Increase the number of wires in parallel.
- Use litz wires.
- Thicken the wire gauge.

● **Current Detection Resistor, R_{OCP}**

It is required to select a current detection resistor with a low internal inductance and high surge capability. A high frequency switching current flows through a detection resistor; therefore, malfunctions may be caused if a resistor with a high internal inductance is used.

9.2. Transformer Design

Figure 9-1 shows an ideal waveform of a sine wave of AC input voltage in the average current control. In the average current control, the IC controls the FB pin voltage to be constant over an AC input voltage, $V_{IN(AC)}$, which is the sine wave of a commercial frequency. Therefore, the envelope curve of the peak drain current, I_{DP}, and the input current, I_{IN} (i.e., average of I_{DP}), becomes sinusoidal, similar to that of the AC input voltage. The values of C6 connected to the FB pin and the secondary-side current detection resistor are adjusted so that the FB pin voltage remains constant.

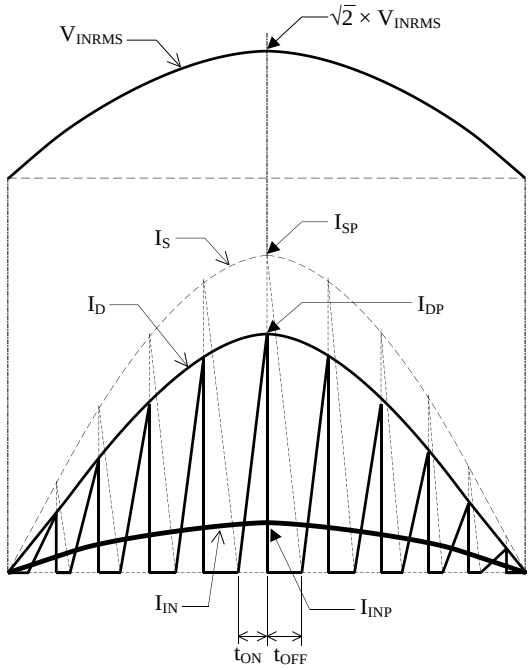


Figure 9-1. Ideal Current Waveform

They symbols in Figure 9-1 are represented as follows:
V_{INRMS} is the effective value (RMS) of a sine wave of AC input voltage,
I_{IN} is the input current,
I_{INP} is the peak input current,
I_D is the power MOSFET drain current,
I_{DP} is the power MOSFET peak drain current,
I_S is the forward current of a secondary side rectifier diode, and
I_{SP} is the peak forward current of a secondary side rectifier diode.

Designing a transformer for the LC5540LD series employs the method for designing ringing choke converter (RCC) transformers. However, a quasi-resonant operation includes a certain delay to a turn-on timing, so duty cycles must be compensated. Moreover, as the input capacitor uses no electrolytic capacitor, the applied voltage of a transformer results in a sine wave of the AC input voltage, $V_{IN(AC)}$, at commercial frequencies. Therefore, the duty cycle compensation for quasi-resonant delay time is added to the basic equation of the RCC topology; moreover, the equation must be changed into the sine wave of the AC input voltage, $V_{IN(AC)}$. Thus, the primary-side inductance, L_P', is expressed as follows:

$$L'_P = \frac{(V_{INRMS(MIN)} \times D_{ON})^2}{\left(\sqrt{\frac{2 \times P_{OUT} \times f_{S(MIN)}}{\eta}} + V_{INRMS(MIN)} \times D_{ON} \times f_{S(MIN)} \times \pi\sqrt{C_V}\right)^2}. \quad (17)$$

Where:

$V_{INRMS(MIN)}$ is the effective value (RMS) of the sine wave of the minimum AC input voltage;
P_{OUT} is the maximum output power calculated by

$$P_{OUT} = V_{OUT} \times I_{OUT}, \text{ where}$$

V_{OUT} is the output voltage, and
I_{OUT} is the maximum output current;

$f_{S(MIN)}$ is the operation frequency at the peak voltage of the sine wave of the AC input voltage (i.e., minimum operation frequency);
η is the efficiency, ranging from 80% to 90%;
C_V is the capacitance of the voltage resonant capacitor (C3), typically rated at between 47 pF and 470 pF;
D_{ON} is the maximum duty cycle not compensated for the quasi-resonant delay time at the sine wave of the minimum AC input voltage, given by

$$D_{ON} = \frac{V_{FLY}}{\sqrt{2} \times V_{INRMS(MIN)} + V_{FLY}}.$$

Where V_{FLY} is the flyback voltage determined by the power MOSFET breakdown voltage and the surge voltage. The power MOSFET breakdown voltage of the IC is defined at 650 V; therefore, the target voltage of V_{FLY} is 100 V to 150 V for universal input specifications.
V_{FLY} is then calculated by

$$V_{FLY} = \frac{N_P}{N_S} \times (V_{OUT} + V_F), \text{ where}$$

N_P is the primary winding,
N_S is the secondary winding, and
V_F is the forward voltage of the secondary rectifier diode, D8 ($V_F \approx 0.7$ V).

The quasi-resonant delay time, t_{ONDLY} is calculated by Equation (18):

$$t_{ONDLY} = \pi\sqrt{L_P' \times C_V}\,. \quad (18)$$

The compensated maximum duty cycle, D_{ON}', which includes a quasi-resonant delay time (t_{ONDLY}) is expressed as:

$$D'_{ON} = \left(1 - f_{S(MIN)} \times t_{ONDLY}\right) \times D_{ON}\,. \quad (19)$$

The RMS input current of the sine wave of the minimum AC input voltage, $I_{INRSM(MAX)}$, is defined as:

$$I_{INRMS(MAX)} = \frac{P_{OUT}}{\eta \times V_{INRMS(MIN)}}\,. \quad (20)$$

The compensated peak drain current, $I_{DP(DLY)}$, is then expressed as:

$$I_{DP(DLY)} = \frac{2\sqrt{2} \times P_{OUT}}{\eta \times D_{ON}' \times V_{INRMS(MIN)}}\,. \quad (21)$$

For proper transformer designing, the following should be taken in to account when you choose the AL-value of a ferrite core used in your transformer: the value of NI-Limit(AT) (= $N_P \times I_{DP(DLY)}$) calculated from the primary winding, N_P, and the peak drain current, $I_{DP(DLY)}$. To avoid transformer saturation, take variations in temperature and in other parameters into account, and choose a ferrite core with a calculated NI-Limit value that ensures a margin of ≥30% to the upper saturation limit defined by the NI-Limit(AT) vs. AL-value graph (i.e., within the hatched area in Figure 9-2):

$$\text{NI-Limit} \leq N_P \times I_{DP(DLY)} \times 130\%\,. \quad (22)$$

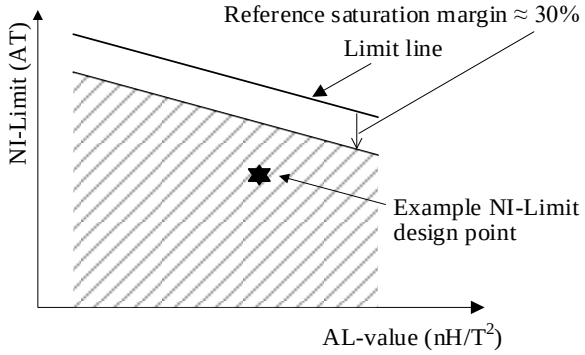


Figure 9-2. Example of NI-Limit vs. AL-value Characteristics

The primary winding (N_P), the secondary winding (N_S), and the auxiliary winding (N_D) are expressed as follows:

$$N_P = \sqrt{\frac{L_P'}{\text{AL-value}}}\,, \quad (23)$$

$$N_S = \frac{V_{OUT} + V_F}{V_{FLY}} \times N_P\,, \text{and} \quad (24)$$

$$N_D = \frac{V_{CC}}{V_{OUT} + V_F} \times N_S\,. \quad (25)$$

9.3. Trace and Component Layout Design

The switching power supply circuit includes high-frequency and high-voltage current paths that affect the IC operation, noise interference, and power dissipation. Therefore, extreme care should be taken when designing traces and component placements on a PCB.

The high-frequency current loops (see Figure 9-3) should be as wide and small as possible to reduce trace impedance. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

Care should be taken in thermal design because the power MOSFET has a positive thermal coefficient of $R_{DS(ON)}$.

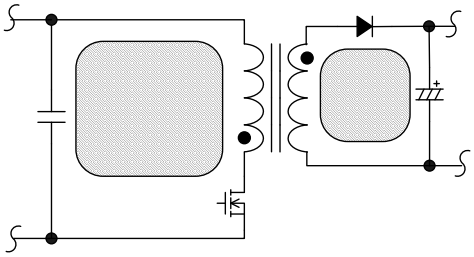


Figure 9-3. High-frequency Current Loops (Hatched Area)

Figure 9-4 is a peripheral circuit example of the IC.

● **IC Peripheral Circuit**

- Traces through the following parts: the S/GND pin, R_{OCP}, C2, T1 (primary winding), and the D/ST pin.
  The switching current flows through these traces. Therefore, these traces should be as wide and short as possible. To reduce the impedance of high-frequency current loops, place an input capacitor, C2, close to the IC or to the transformer.
- Traces through the following parts: the S/GND pin, C4 (–), T1 (auxiliary winding, D), R1, D5, C4 (+), and the VCC pin
  These traces are used for supplying voltage with the IC. Therefore, these traces should be as wide and short as possible.
  If the IC and C4 are distant from each other, place a film or ceramic capacitor of 0.1 µF to 1.0 µF between the VCC and S/GND pins with a minimal length of traces.
- R_{OCP}
  R_{OCP} should be placed as close as possible to the S/GND pin.
  In addition, to avoid the conditions in which the common impedance of traces or the switching current will negatively affect the control circuit, connect the trace of R3 to the base of R_{OCP} at point A in Figure 9-4.

● **Secondary Rectifier Smoothing Circuit: Traces through T1 (secondary winding), D8, and C9**

Since the secondary-side switching current flows through these traces, they should be as wide and short as possible. If the traces are thin and long, a surge voltage at power MOSFET turn-off becomes high due to increased parasitic leakage inductance on traces. Therefore, a proper secondary layout permits your application to have an increased margin to the power MOSFET breakdown voltage and reduced component stress and loss in the clamp snubber circuit.

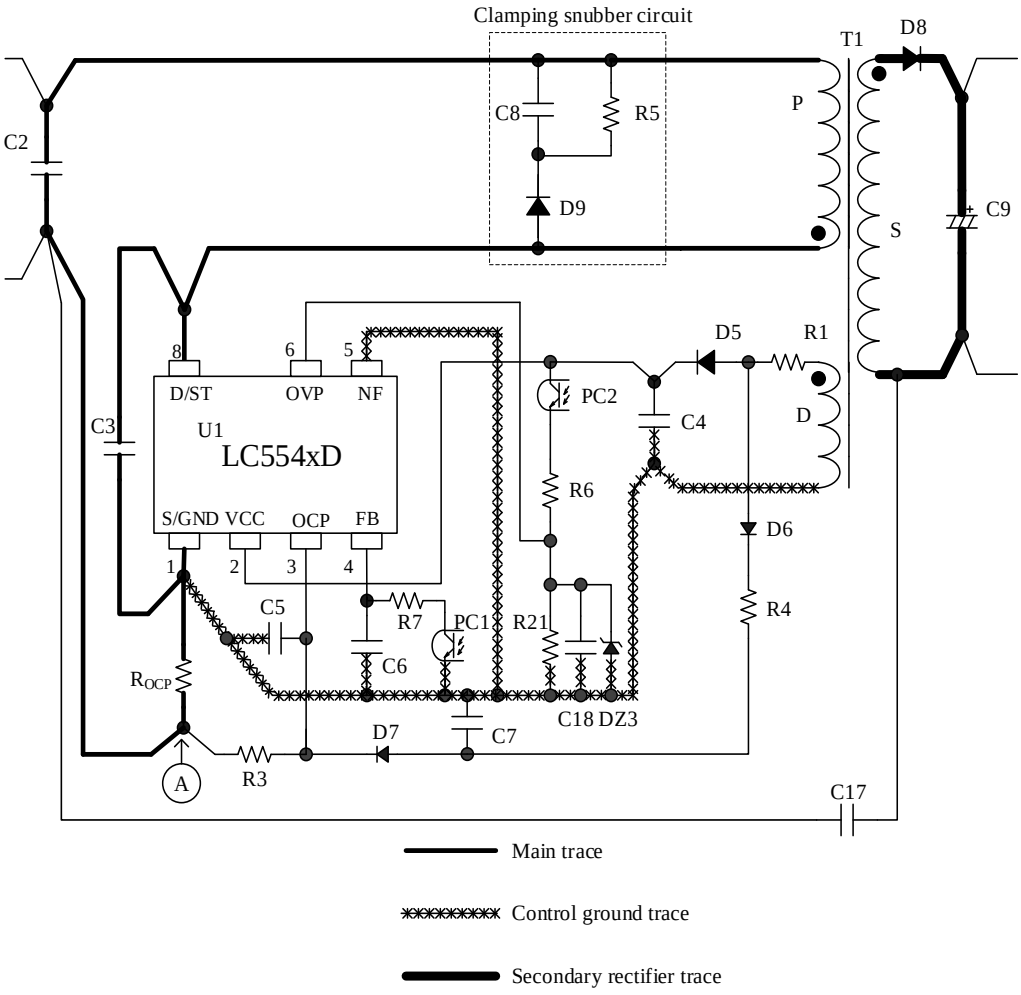


Figure 9-4. Peripheral Circuit Example around the IC

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